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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	PAPER NUMBER
2638	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/827,306	BUSSON ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 11-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Ciccarelli et al U.S. patent No 6,498,926 B1.

As per claim 11, process for controlling a tuner having a zero intermediate frequency and comprising an analog circuit, a digital circuit, and an analog/digital conversion stage connected there between, the analog circuit comprising a frequency transposition stage and a first controlled-gain amplifier stage connected upstream (see figs. 2-4) thereof the process comprising: calculating an overall power (see fig.2-3 element 1290 or 1390 and col.12, lines 11-40) of an entire signal having a plurality of channels (see fig.4 element I and Q and col.7, lines 18-28) received by the tuner during a phase initialization; comparing the calculated overall power the digital circuit with a first reference value corresponding to desired power at a predetermined location in the analog circuit (see col.12, lines 39-67 and col.15, lines 1-25); adjusting a gain of first controlled-gain amplifier stage based upon a deviation between the calculated overall power and the first reference value (see fig.2 element 1280 and col.6,lines 54-60 and

col.7, lines 53-57); and selecting one of the plurality of channels during a phase of normal operation after the gain of the first controlled-gain amplifier stage has been adjusted (see col.8, lines 23-25 and col.17, lines 1-5).

As per claim 12, Ciccarelli et al does teach calculating the overall power comprises mean power (see fig.2 element 1290 and col.12, line 13).

As per claim 13, Ciccarelli et al does teach desired power at the predetermined location receiver is a maximum power (see col.12, line 13-67).

As per claims 14, 25, 36 Ciccarelli et al does teach, wherein the gain of the first controlled-gain amplifier stage is adjusted to minimize (see col.12, lines 48-55) the deviation between the calculated overall power and the first reference.

As per claim 15, Ciccarelli et al does teach, wherein the analog circuit further comprises a base band filter (see figs.2 element 1232 and col.7, line 33) connected to an output the frequency transposition stager (see fig.2 element 1230) and a second controlled-gain amplifier (see fig.2 element 1234) stage connected an output of the base band filter; and the process further comprising: calculating a channel power of the selected channel during the phase of normal operation (see fig.2-3 element 1290 or 1390 and col.12, lines 11-40); comparing (see col.12, lines 39-67 and col.15, lines 1-25) the calculated channel power second reference value corresponding a desired channel power desired at an input of the analog/digital conversion stage; adjusting a gain(see col.8, lines 23-25 and col.17, lines 1-5) of the second controlled-gain amplifier stage based upon a deviation between the calculated channel power and the second reference value.

As per claims 16, 23 Ciccarelli et al does teach, wherein comprises calculating a mean power (see fig.2-3 element 1290 or 1390 and col.12, lines 11-40).

As per claims 17, 24, 35 Ciccarelli et al does teach desired power at the predetermined location receiver is a maximum power (see col.12, line 13-67).

As per claims 18, Ciccarelli et al does teach, wherein the gain of the second controlled-gain amplifier stage is adjusted to minimize (see col.12, lines 48-55) the deviation between the calculated overall power and the first reference.

As per claims 19, 31 Ciccarelli et al does teach wherein calculating the overall power of the entire signal is based upon signal available between an output of the first controlled-gain amplifier stage and an input of the frequency transposition stage (see fig.2-3 element 1290 or 1390 and col.12, lines 11-40).

As per claim 20, Ciccarelli et al does teach wherein calculating the overall power of the entire signal is performed in the digital circuit (see fig.2 element 1290).

As per claim 21, Ciccarelli et al does teach, wherein the controlled-gain amplifier stage comprises an attenuator for attenuating the signal (see fig.2 element 1216 and col.7, line 47).

As per claims 22, Ciccarelli et al does teach a process for controlling a tuner having zero intermediate frequency and comprising an analog circuit, a digital circuit, and an analog/digital conversion stage connected there-between, the analog circuit comprising first controlled-gain amplifier stage and a second controlled-gain amplifier stage with a frequency transposition stage connected there-between the process comprising (see figs. 2-4): calculating an overall power an entire signal having a plurality

of channels received by the tuner during phase of initialization(see fig.2-3 element 1290 or 1390 and col.12, lines 11-40); adjusting a gain of the first controlled-gain amplifier stage based upon a deviation between the calculated overall power and a first reference value corresponding desired power a predetermined location in the analog circuit(see fig.2 element 1280 and col.6,lines 54-60 and col.7, lines 53-57); selecting one of the plurality channels during a phase of normal operation after the gain of the first controlled-gain amplifier stage has been adjusted (see col.8, lines 23-25 and col.17, lines 1-5); calculating a channel power of the selected channel during the phase of normal operation (see fig.2-3 element 1290 or 1390 and col.12, lines 11-40); and adjusting a gain second controlled-gain amplifier stage based upon a deviation between the calculated channel power and a second reference value corresponding to a) desired channel power at an input of the conversion stage (see figs 2-3 elements 1280,1380 and col.8, lines 23-25 and col.17, lines 1-5).

As per claims 26, 30, Ciccarelli et al does teach, wherein adjusting the gain the first controlled-gain amplifier stage comprises comparing calculated overall power the first reference value (see col.12, lines 38-67).

As per claims 27, 34, Ciccarelli et al does teach wherein calculating the channel power comprises calculating a mean channel power (see col.12, lines 38-67).

As per claims 28, 32, 35 Ciccarelli et al does teach wherein the desired channel power at the input of the analog/digital conversion stage is a maximum channel power (see col.12, lines 38-67).

As per claim 29, Ciccarelli et al does teach wherein second controlled-gain amplifier stage is adjusted (see col.12, lines 38-67).

As per claims 33, 46, Ciccarelli et al does teach tuner having a zero intermediate frequency and comprising: an analog circuit comprising a first controlled-gain amplifier (see figs 2-3 element 1220a, 1320a) stage having an input receiving an entire signal having a plurality of channels; a signal routing circuit (see fig.2 element 1224) having an input receiving the entire signal from said controlled-gain amplifier stage, and a frequency transposition stage (see fig.2 element 1230) connected to first output of said signal routing circuit; an analog/digital conversion stage having an input being connected to an output of said frequency transposition stage or to a second output of said signal routing circuit (see fig.4 element 1410); a digital circuit connected to said analog/digital conversion stage and comprising a first adjustment circuit for adjusting a gain of said first controlled-gain amplifier stage based upon comparing a calculated overall power of the entire signal with a first reference value corresponding to a desired power at a predetermined location in said analog circuit(see fig.2-3 element 1290 or 1390 and col.12, lines 11-67 and col.15, lines 1-25); and a control circuit connected to said signal routing circuit for connecting the input to the second output thereof for adjusting (see fig.2 element 1280 and col.6,lines 54-60 and col.7, lines 53-57) a deviation between the calculated overall power and the first reference value during a phase of initialization, and for connecting the input to the first output thereof for selecting (see col.8, lines 23-25 and col.17, lines 1-5) one of the plurality of channels during a

phase of normal operation after the gain of said first controlled-gain amplifier stage has been adjusted.

As per claims 37, 47, 50 Ciccarelli et al inherently teaches wherein said digital circuit further comprises: first calculator circuit for providing the calculated overall power; and first comparison circuit for comparing the calculated overall power with the first reference value.

As per claims 38, 51 Ciccarelli et al inherently teaches further base band filter connected to an output of said frequency stage.

As per claims 39, 52 Ciccarelli et al teaches wherein said a second controlled-gain amplifier stage (see fig.2 element 1234) connected an output of said frequency transposition stage.

As per claims 40, 49, Ciccarelli et al inherently teaches wherein said digital circuit further comprises a second adjustment circuit for adjusting of said second controlled-gain amplifier stage based upon a deviation between a calculated channel power of a selected channel and a second reference value.

As per claims 41, 48, 55, 57 Ciccarelli et al inherently teaches calculated channel power comprises a mean 40, wherein the channel power.

As per claim 42, Ciccarelli et al inherently teaches wherein the gain of said second controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated channel power and the second reference value.

As per claims 43, 53, 56 Ciccarelli et al inherently teaches wherein said digital circuit further comprises: a second calculation circuit for providing calculated channel

power during a phase of normal operation; and a second comparison circuit comparing the calculated channel power with the second reference value corresponding desired channel power at an input of said analog/digital conversion stage.

As per claim 44, Ciccarelli et al inherently teaches, wherein the desired channel power maximum channel power.

As per claim 45, Ciccarelli et al inherently teaches, further comprising a semiconductor substrate such that said analog circuit, said analog/digital conversion stage, and said digital circuit are integrated on said semiconductor substrate.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gurantz et al U.S. patent No 5,550,869 teaches a demodulator.

Luz et al U.S. patent No 6,231,073 B1 teaches a radiotelephone.

Swanke et al U.S. patent No 6,477,196 B1 teaches a direct sequence spread spectrum.

Dowling U.S. Patent No 6,434,186 B2 teaches a priority channel search.

Cho et al U.S. Patent No 6,208,849 B1 teaches a receiver.

Wheatley, III U.S. patent No 5,732,341 teaches a method and apparatus for increasing receiver immunity to interference.

Black U.S. patent No 6,181,201 B1 teaches an AGC

Mohindra U.S. Patent No 6,442,380 B1 teaches an AGC.

Nagano et al U.S. Patent No 6,011,980 teaches wireless telecommunication equipment.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vanderpuye Kenneth can be reached on 571 272 3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2638

7/22/05